REMARKS

The specification has been amended to correct additional inadvertent errors. No new matter is believed to have been added.

The specification and the drawings have been objected to for introducing new matter. Claims 1-20 are also rejected under 35 U.S.C. § 112, first paragraph, as being drawn to new matter.

The formula on page 15, lines 17-18 of the specification is amended read "PE= (Y_t-Y_{t-1}) X $hat_{t,\ t-1} - (Y_{t-1} - Y_{t-2})$ X $hat_{t-1,\ t-2}$". This amendment is supported by the original disclosure, namely the original claim 2, which recites that

> "the readout signal successively comprises a first, a second and a third sampled value in an order sampled, and said phase error calculation circuit calculates the phase error based on a difference between an absolute value of a difference between the first and second sampled values and an absolute value of a difference between the second and third sampled values."

The features of original claim 2 which were canceled after filing are incorporated in previously amended claims 1 and 19. Further support is found on page 16, lines 18-26 of the specification, where it is described that

> "the subtracter 339 uses the absolute values of the two first differences, which are calculated by multiplying each of the two first differences by the ternary code "hat" to correct the transition direction, so as to calculate the difference between the two absolute values from the above equation (a second difference), which is equal to the phase error of the clock signal".

Accordingly, "hat" obtains the absolute value of (Y_t-Y_{t-1}), and it is evident that (Y_t-Y_{t-1}) X $\underline{hat_{t,\ t-1}}$ is the correct term, and that (Y_{t-1}, Y_{t-2}) X $\underline{hat_{t-1,\ t-2}}$ is the correct term for similar reasons.

It is believed that the amendments on page 17, lines 5-9 and page 18, lines 8-9 also include no new matter for the similar reasons.

With regard to the amendments on page 17, lines 5-9, it is evident from FIG. 5 and the description on page 16, line 27 to page 17, line 9 that "PE = $\underline{(0\text{-}1)\ X\ (\text{-}1) - (1\text{-}2)}$ X (-1)" is the correct expression.

The amendments to FIG. 4 is in line with the formula describing the phase error PE. More particularly, the output of the code determination circuit 335 is input to the multiplier 337 which computes the term (Y_t-Y_{t-1}) X $\underline{hat_{t,\ t-1}}$, and the output of the code determination circuit 336 is input to the multiplier 338 which computes the term (Y_{t-1}, Y_{t-2}) X $\underline{hat_{t-1,\ t-2}}$. The amendments on page 16, lines 6 and 13 correctly describe the process of computing the phase error PE, in line with the amendments to FIG. 4.

Claims 1-17 stand rejected under the doctrine of obviousness-type double patenting as being unpatentable over claims 1, 2, 3 and 10 of Hamada et al. (U.S. Pat. No. 6,151,282) in view of a number of secondary references. A Terminal Disclaimer is submitted herewith with respect to Patent No. 6,151,282 to overcome the double patenting rejection. Withdrawal of the rejection is respectfully requested.

Claims 1, 3-8, 11, 13 and 17-20 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Tsuchinaga. Applicants respectfully traverse this rejection because, the

cited reference does not disclose or suggest calculating the phase error based on the difference between first and second sample values and the difference between the second and the third sample values of consecutive first, second and third sample values of the readout signal, as in the present invention.

The Examiner asserts that the claimed phase error calculation circuit is disclosed by Figs. 4, 7, 9 and 10, and column 18, lines 40-46, since they show three consecutive samples. The figures referred to by the Examiner relate to an intermediate value decider 205 or the equalizer 203, and not a phase error detector, which is shown as reference numeral 207 in Fig. 2 of the reference. Tsuchinaga teaches that the phase error detector 207 outputs a phase error based on sampling timings with respect to a reference level, as shown in Fig. 6 and its corresponding description in col. 7, line 27-col. 8, line 2. It does not disclose or suggest calculating the phase error based on the difference between first and second sample values and the difference between second and third sample values of consecutive first, second and third sample values of the readout signal, as in the present invention. In other words, Tsuchinaga merely obtains the phase error based on an error of one sample from a reference level. However, the present invention does not use a reference level, and obtains the phase error using three samples. For this reason, the present invention as described in independent claims 1, 18 and 19, and their dependent claims 2-17 and 20 are believed to be allowable.

Claims 1, 2, 4-8 and 19-20 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Fujimoto. Applicants respectfully traverse this rejection, because the

Fujitmoto reference also does not disclose or suggest calculating the phase error based on the difference between the first and second sample values and the difference between the second and third values of consecutive first, second and third sample values of the readout signal, as described in claims 1 and 19, and now also in claim 18.

Fujimoto teaches that the phase-error detecting circuit 6 detects a transition of the second interpolation value of the playback signal fed back thereto by a second interpolation circuit 4 from positive to negative or vice versa which is known as an interpolation-value zero cross. A zero-cross timing is then used for generating a phase-error signal which is output to a loop filter 7 (see col. 6, lines 42-50). Clearly, Fujimoto also does not disclose or suggest calculating the phase error based on the difference between first and second sample values and the difference between second and third samples values of consecutive first, second and third sample values of the readout signal, as in the present invention. In other words, Fujimoto merely obtains the phase error at a zero-crossing position by observing the change in the sample value. However, the present invention does not use a zero-crossing (or reference level), and obtains the phase error using three samples. For this reason, the present invention is believed to be allowable.

Claim 18 stands rejected under 35 U.S.C. § 102(e) as being anticipated by, or in the alternative, under 35 U.S.C. § 103(a) as being obvious over Yamaguchi et al. Applicants respectfully traverse this rejection, because the Yamaguchi et al. also does not disclose or suggest calculating the phase error based on the difference between the first and second

sample values and the difference between the second and third sample values of consecutive first, second and third sample values of the readout signal, as in the present invention.

Even assuming that the Yamaguchi et al. discloses that the phase error is calculated based on the transition states, as asserted by the Examiner, it still does not disclose or suggest calculating the phase error based on the absolute values of the differences of three different sample values, as now described in claim 18. For this reason, claim 18 is now also believed to be allowable.

All or some of dependent claims 2-17 and 20 stand rejected based on §102 or 103. These claims are allowable for the same reasons given with respect to their independent claims 1 and 19, and for the additional features recited in these dependent claims.

For all of the above reasons, Applicants request reconsideration and allowance of the claimed invention. The Examiner should contact Applicants' undersigned attorney if a telephone conference would expedite prosecution.

Respectfully submitted,

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